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10/808,225	03/23/2004	Robert P. Masleid	TRAN-P249	5029

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,225	MASLEID ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-39,41-65,67-71,73 and 74* is/are pending in the application.

4a) Of the above claim(s) *32-38,41,47-62,68 and 74* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39,42-46,63-65,69-71 and 73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 27, 2008 has been entered.

Status of the Claims

2. Amendment filed March 27, 2008 is acknowledged. Claims 39, 65, 67 and 69 have been amended. Claims 40, 66 and 72 have been cancelled. Claims 32-39, 41-65, 67-71, 73 and 74 are pending. Non-elected invention and species, claims 32-38, 41, 47-62, 68 and 74 have been withdrawn.

Action on merits of Claims 39, 42-46, 63-65, 69-71 and 73 follows.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

DEEP WELL REGIONS FOR ROUTING BODY-BIAS VOLTAGE TO MOSFETS IN SURFACE WELL REGIONS HAVING SEPARATION WELLS OF P-TYPE BETWEEN THE SEGMENTED DEEP N WELLS.

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claim 39 recites: "wherein a **doping concentration of said separation well is greater than said p-type material substantially surrounding said deep n well**".

The above does not have antecedent basis in the specification.

Claim Objections

5. Claims 42-45 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

With respect to claim 42, the limitation: "deep n well is parasitically coupled to said principle operating voltage" has already been claimed in claim 39.

With respect to claims 43 and 44, the limitation "p-type material comprises **epitaxy** (claim 43) or **bulk p material** (claim 44)" are product-by-process limitation thus, fails to further limit "p-type material" already claimed in claim 39.

With respect to claim 45, the limitation "p-type material comprises a p well" fail to further limit "p-type material" of claim 39 because what or how the material is being used does not physically alter the p-type material.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 39, 42-46, 63-65, 69-71 and 73 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "wherein a **doping concentration** of *said separation well* is **greater than said p-type material substantially surrounding said deep n well**" in the application as filed. (Emphasis added).

At best, the specification on page 8, first paragraph states: it is appreciated that **separation p well 290 is not required**.

Applicant must cancel the new matters.

7. Claim 46 is further rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 46 recites: wherein said p well is at **substantially a same depth** as said deep n well.

As shown in Fig. 1, the NFET is formed in p well (on the right). This p well is formed above the deep n wells 230, 240.

How can p well formed above the deep n well be characterized as same depth ?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 67 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 67 fails to depend on any claim, thus claim 67 is indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 69-71 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (US Patent No. 5,508,549).

With respect to claim 69, Watanabe teaches an integrated circuit as claimed including:

one or more wells (5) of a first conductivity type;

one or more wells (50) of a second conductivity type;

a first plurality of transistors (61) within the one or more wells (5) of the first conductivity type;

a second plurality of transistors (62) within the one or more wells (50) of the second conductivity type;

a deep well (2) of a second conductivity type disposed between one or more wells (5) of the first conductivity type and a substrate (1) of first conductivity type, wherein the deep well (2) includes a plurality of substructures having a plurality of gaps wherein the one or more wells (5) of the first conductivity type are coupled to the substrate (1); and

a separation well (40) of the first conductivity type disposed within one or more of the gaps and coupling the one or more wells (5) of the first conductivity type to the substrate (1), wherein the doping concentration of the separation well (40) is greater than the one or more wells (5) of the first conductivity type and the substrate (1). (See Fig. 14).

With respect to claim 70, a principal operating potential (106) of Watanabe is coupled between the deep well (2) and the substrate (1).

With respect to claim 71, deep well (2) of Watanabe is further disposed between the one or more wells (50) of second conductivity type and the substrate (1), and wherein the deep well (2) further includes a plurality of substructures having a second plurality of gaps (40) wherein one or more wells (50) of the second conductivity type are adjacent to the substrate (1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 39, 42-46, 63-65, 67 and 69-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr (U.S. Patent No. 6,586,817) of record in view of Watanabe '549.

With respect to claim 39, Burr teaches an integrated circuit substantially as claimed including:

a plurality of transistors (701; 702) having a principal operating voltage (Vnw);

a deep n well capacitor structure comprising:

a deep n well (770) segmented into a plurality of substructure proximate each one of the plurality of transistors, wherein n-type material of the deep n well is coupled to the principal operating voltage (Vnw);

p-type material (706) substantially surrounding the deep n well (770) and coupled to the ground reference (Vpw); and

a separation well (790A, B) disposed between the plurality of substructures (770) and between the p-type material (706) beneath the deep n-well (770) and above the deep n-well. (See Fig. 7C).

Thus, Burr is shown to teach all the features of the claim with the exception of explicitly disclosing the doping concentration of the separation well (790A,B) being greater than that of the p-type material (706) surrounding the deep n well.

However, Watanabe teaches an integrated circuit including separation well (40) disposed between the plurality of substructures (2) and having a doping concentration greater than that of the p-type material (1, 5) surrounding the deep n well (2). (See Fig. 14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the separation well of Burr having doping concentration greater than the p-type material surrounding the deep n well as taught by Watanabe to provide the conduction path at a lower resistance.

With respect to claim 42, the deep n well (770) of Burr is parasitically coupled to the principal operating voltage (Vnw).

With respect to claim 43, the p type material of Burr comprises epitaxy.

Product by process limitation:

The expression "epitaxy" (claim 43) or "bulk" (claim 44) is/are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that Applicant has burden of proof in such cases as the above case law makes clear.

With respect to claim 44, the p type material of Burr comprises bulk p material.

With respect to claim 45, the p type material of Burr comprises a p well.

With respect to claim 46, the p well of Burr is at substantially a same depth as said deep n well (770).

With respect to claim 63, the deep n well capacitor structure of Burr has a surface area selected to provide a specified amount of decoupling capacitance between one or more of the plurality of transistors and the principal operating voltage. (Same structure same function).

With respect to claim 64, the plurality of gaps (790A, B) between the pluralities of substructures of Burr does not close under bias conditions.

With respect to claim 65, the plurality of substructures (770s) of Burr provides connectivity between the p-type material (706B) beneath the deep n-well (770) and above (706A) the deep n-well.

With respect to claim 67, as best understood by Examiner, in view of Watanabe, the separation well increases coupling between said p-type material (706B) beneath the deep n-well (770) and above (706A) the deep n-well.

With respect to claim 69, Burr teaches an integrated circuit substantially as claimed including:

one or more wells (706A) of a first conductivity type;

one or more wells (711) of a second conductivity type;

a first plurality of transistors (701) within the one or more wells (706A) of the first conductivity type;

a second plurality of transistors (702) within the one or more wells (711) of the second conductivity type;

a deep well (770) of a second conductivity type disposed between one or more wells (706A) of the first conductivity type and a substrate (706B) of first conductivity type, wherein the deep well (770) includes a plurality of substructures (770s) having a plurality of gaps (790A,B) wherein the one or more wells (706A) of the first conductivity type are coupled to the substrate (706B); and

a separation well (790A, B) of the first conductivity type disposed within one or more of the gaps and coupling the one or more wells (706A) of the first conductivity type to the substrate (706B). (See Fig. 7C).

Thus, Burr is shown to teach all the features of the claim with the exception of explicitly disclosing the doping concentration of the separation well (790A,B) being greater than that of the one or more wells of the first conductivity type and the substrate.

However, Watanabe teaches an integrated circuit including separation well (40) disposed within one or more of the gaps and coupling the one or more wells (5) of the first conductivity type to the substrate, wherein the doping concentration of the separation well (40) is greater than the one or more wells (5) of the first conductivity type and the substrate (1). (See Fig. 14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the separation well of Burr having doping concentration greater than the one or more wells of the first conductivity type and the substrate as taught by Watanabe to provide the conduction path at a lower resistance.

With respect to claim 70, a principal operating potential (Vnw) of Burr is coupled between the deep well (770) and the substrate (706B).

With respect to claim 71, deep well (770) of Burr is further disposed between the one or more wells of second conductivity type (711) and the substrate (706B), and wherein the deep well (770) further includes a plurality of substructures (perforated 770) having a second plurality of gaps (790A,B) wherein one or more wells (711) of the second conductivity type (N) are adjacent to the substrate (706B).

11. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burr '817 and Watanabe '549 as applied to claim 69 above, and further in view of Williams et al. (US Patent No. 6,900,091) of record.

Burr and Watanabe are shown to teach all the features of the claim with the exception of explicitly further comprises additional wells of first and second conductivity type and a second deep well of second conductivity type such that the additional wells of the first conductivity type are isolated from the substrate by the second deep well.

However, Williams teaches an integrated circuit aside from deep well (152b) of a second conductivity type having plurality gaps, also includes:

one or more additional wells (154b) of first conductivity type;

one or more additional wells (153a) of second conductivity type; and

a second deep well (152a) of second conductivity type disposed between one or more additional wells (154b; 153a) of first and second conductivity type and

the substrate (151), wherein the one or more additional wells (154b) of first conductivity type are isolated from the substrate (151) by the second deep well (152a). (See Fig. 7A).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the integrated circuit of Burr, in view of Watanabe, to further include the isolated well of the first conductivity type as taught by Williams so that the devices operating at different voltages can be integrated into a same substrate without interfering with the functionality of other device, hence integrated circuit.

12. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe '549 as applied to claim 69 above, and further in view of Williams '091.

Watanabe is shown to teach all the features of the claim with the exception of explicitly further comprises additional wells of first and second conductivity type and a second deep well of second conductivity type such that the additional wells of the first conductivity type are isolated from the substrate by the second deep well.

However, Williams teaches an integrated circuit aside from deep well (152b) of a second conductivity type having plurality gaps, also includes:

one or more additional wells (154b) of first conductivity type;

one or more additional wells (153a) of second conductivity type; and

a second deep well (152a) of second conductivity type disposed between one or more additional wells (154b; 153a) of first and second conductivity type and the substrate (151), wherein the one or more additional wells (154b) of first

conductivity type are isolated from the substrate (151) by the second deep well (152a). (See Fig. 7A).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the integrated circuit of Watanabe to further include the isolated well of the first conductivity type as taught by Williams so that the devices operating at different voltages can be integrated into a same substrate without interfering with the functionality of other device, hence integrated circuit.

Response to Arguments

13. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Anh D. Mai/
Primary Examiner, Art Unit 2814